FIG. 1

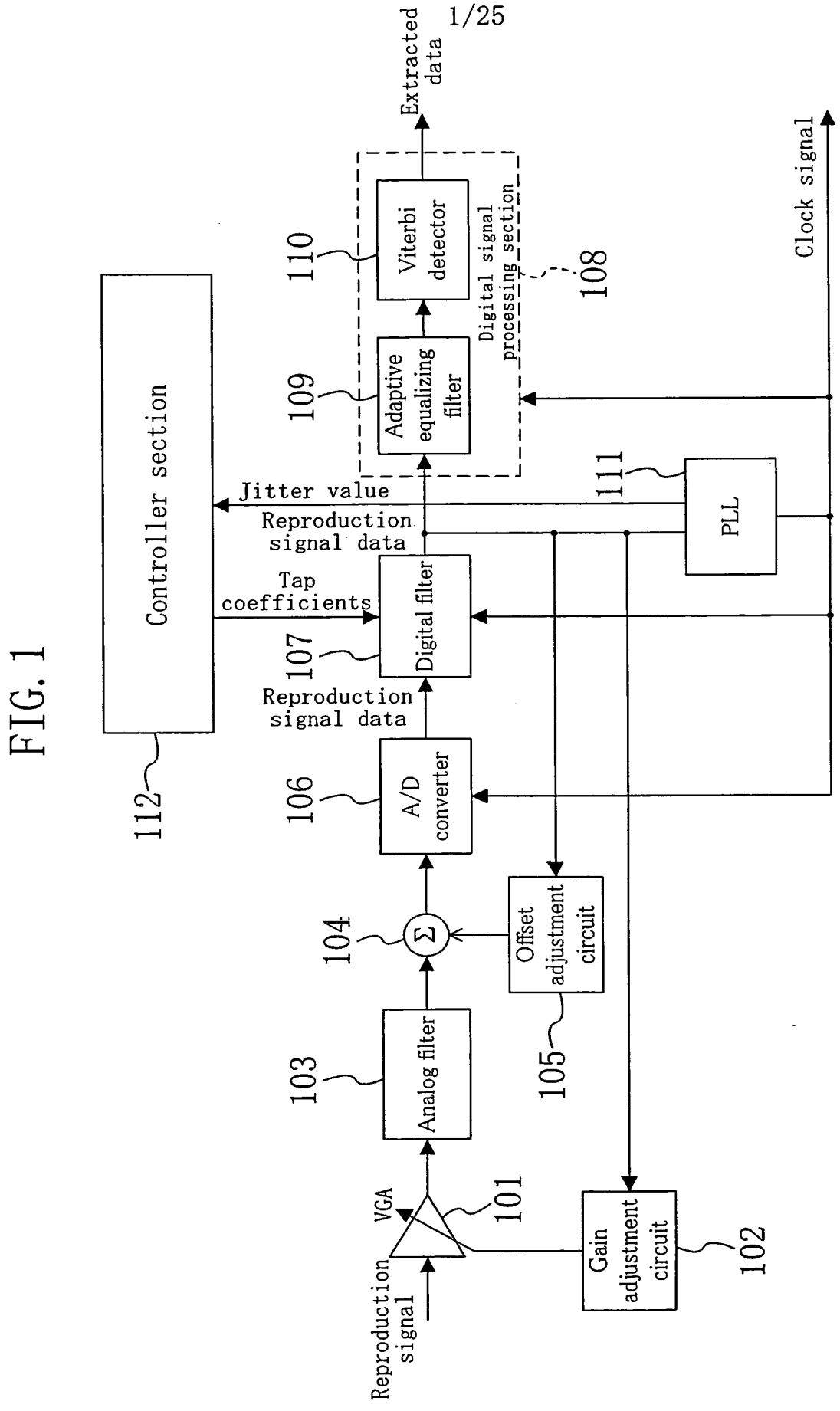

Extracted data
Viterbi detector
110
Digital signal processing section
108
Clock signal
Adaptive equalizing filter
109
Controller section
Jitter value
Reproduction signal data
111
PLL
Tap coefficients
Digital filter
107
Reproduction signal data
A/D converter
106
112
Σ
104
Offset adjustment circuit
Analog filter
103
105
VGA
101
Gain adjustment circuit
102
Reproduction signal

FIG. 2

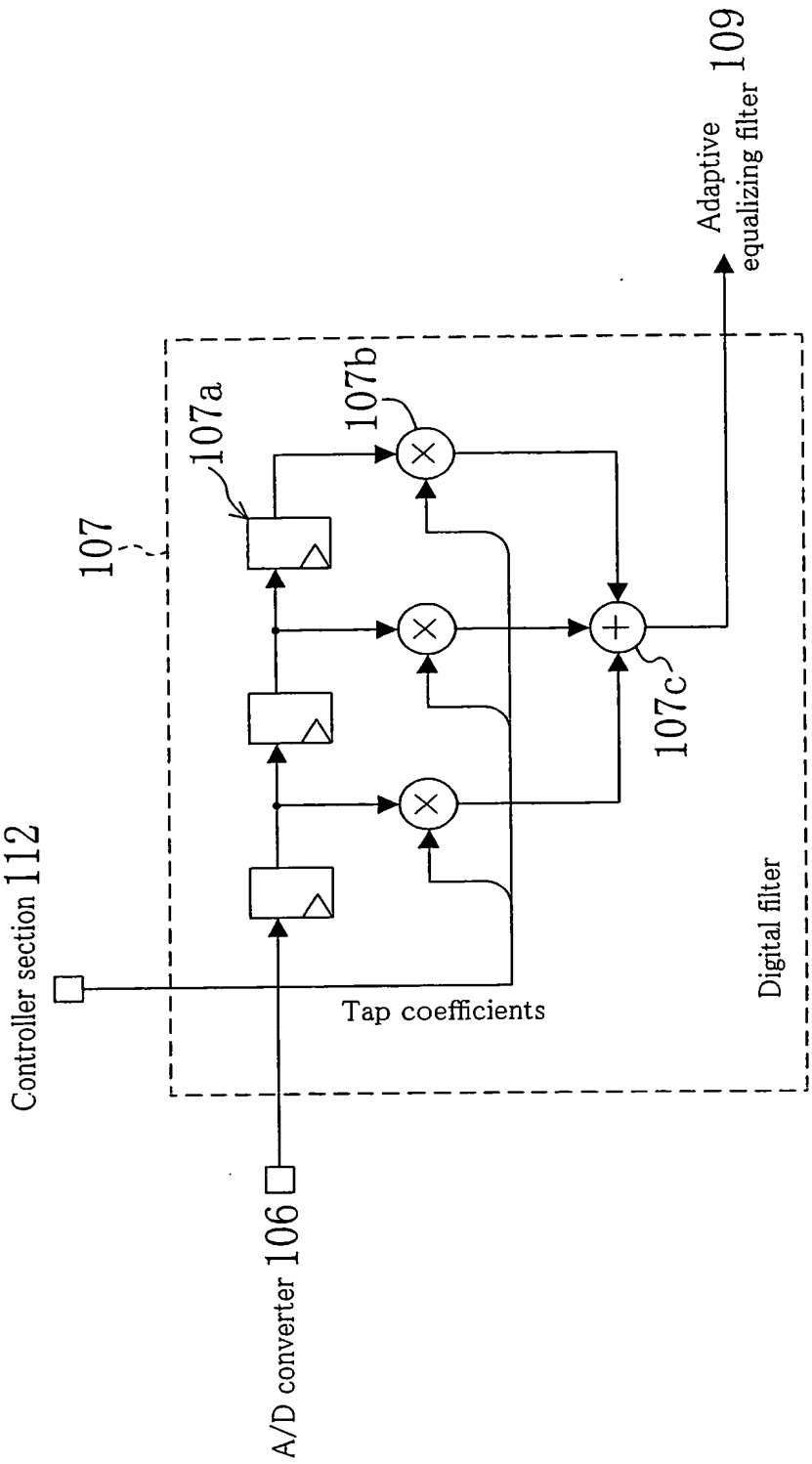

Adaptive equalizing filter 109
107
107a
107b
107c
Controller section 112
Tap coefficients
Digital filter
A/D converter 106

FIG. 3

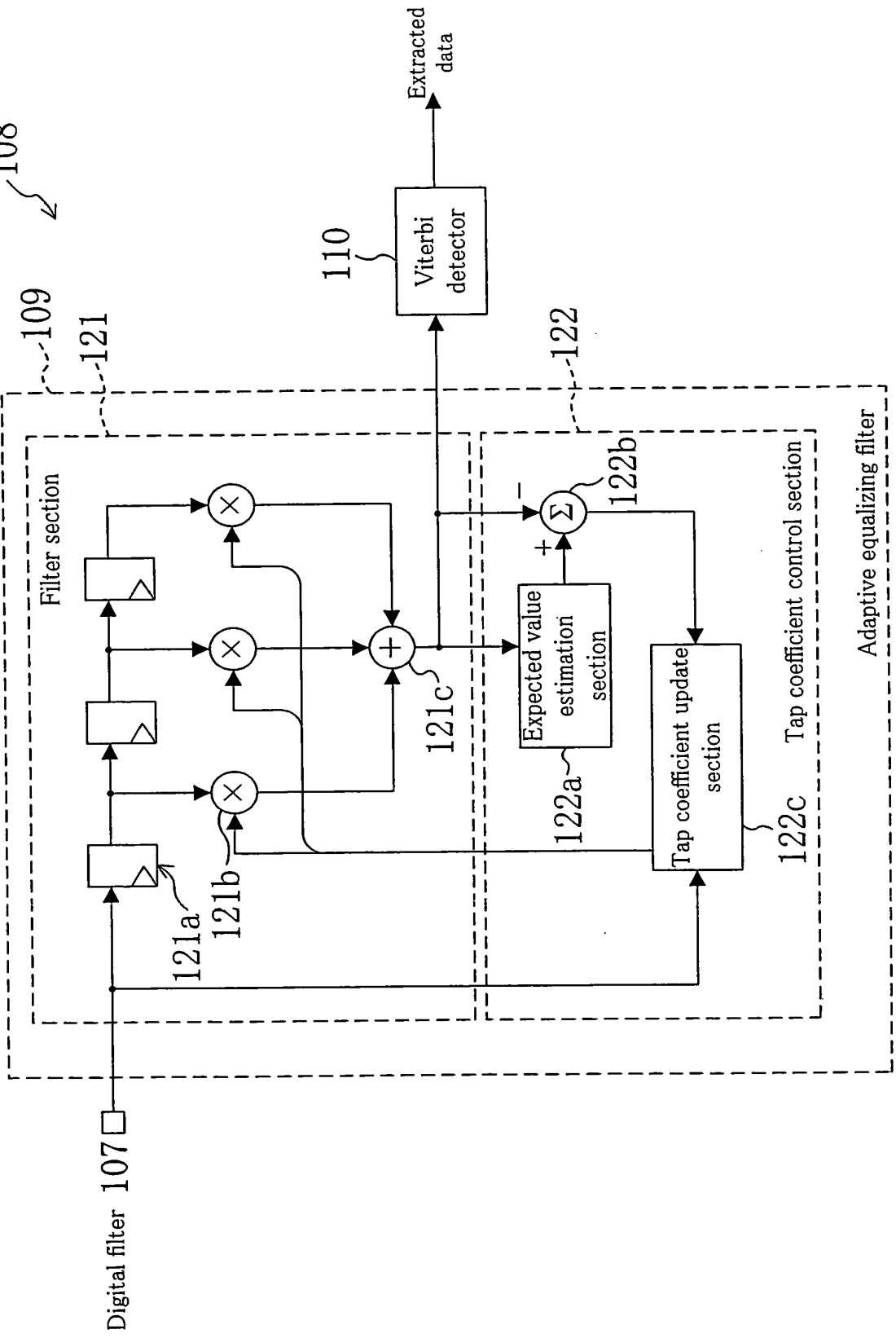

108
109
121
122
Extracted data
110
Viterbi detector
Filter section
Adaptive equalizing filter
Tap coefficient control section
Digital filter
107
121a
121b
121c
122a
122b
122c
Expected value estimation section
Tap coefficient update section
Σ
+
−

FIG. 4

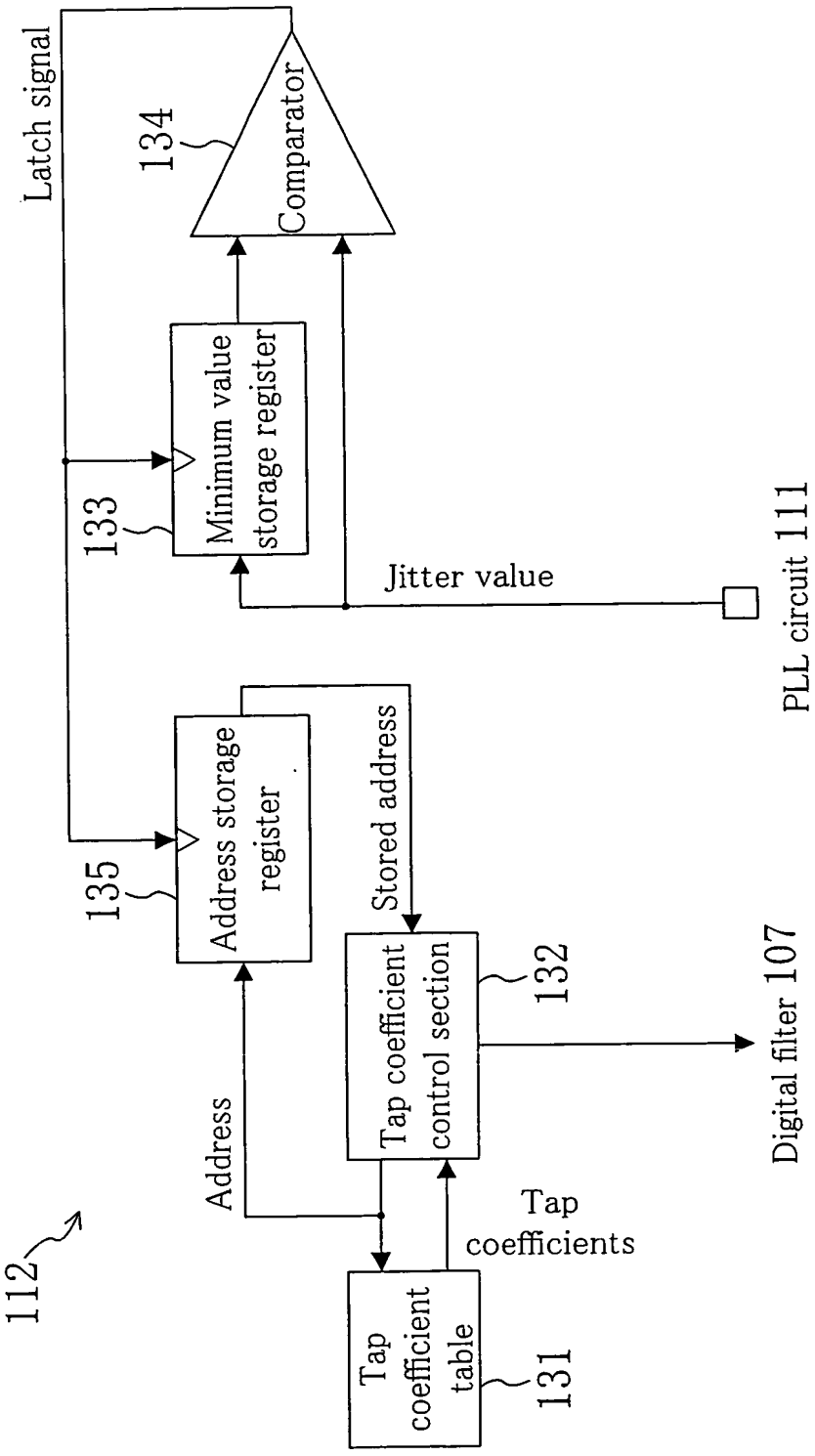

Latch signal
134
Comparator
133
Minimum value storage register
Jitter value
PLL circuit 111
135
Address storage register
Stored address
Tap coefficient control section
132
Digital filter 107
Address
Tap coefficients
112
Tap coefficient table
131

FIG. 5

Tap coefficient table 131

Combinations of cutoff characteristic and boost characteristic	Tap position	Storage address	Data value (tap coefficient)
Cutoff fc1 Boost b0	Tap 1	00	-5
	Tap 2	01	10
	Tap 3	02	-5
Cutoff fc2 Boost b0	Tap 1	03	-3
	Tap 2	04	13
	Tap 3	05	-3
Cutoff fc3 Boost b0	Tap 1	06	-2
	Tap 2	07	15
	Tap 3	08	-2
Cutoff fc1 Boost b1	⋮	⋮	⋮

FIG. 6

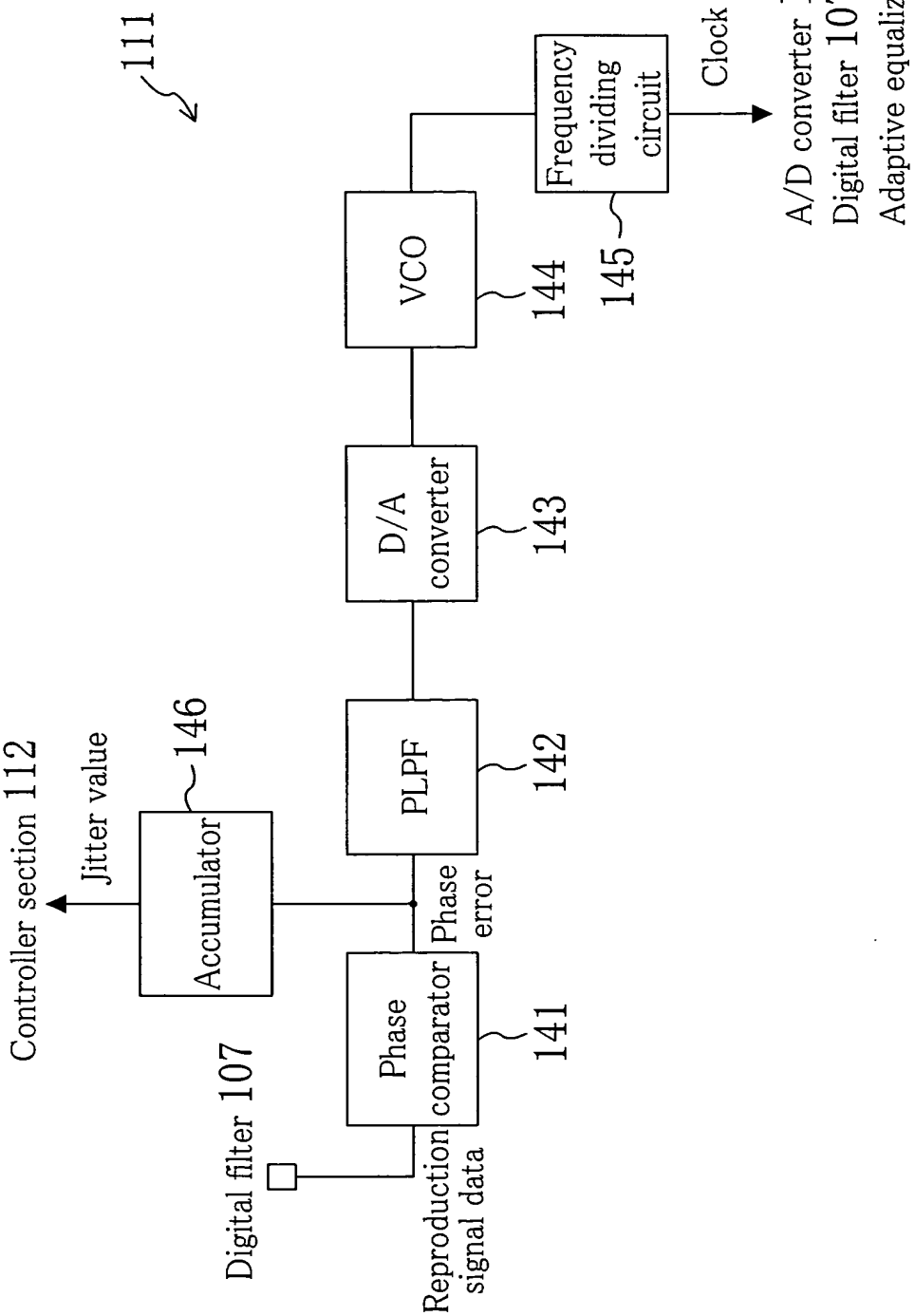

111
Controller section 112
Jitter value
146
Accumulator
Digital filter 107
Phase comparator
141
Reproduction signal data
Phase error
PLPF
142
D/A converter
143
VCO
144
Frequency dividing circuit
145
Clock signal
A/D converter 106
Digital filter 107
Adaptive equalizing filter 109

FIG. 7

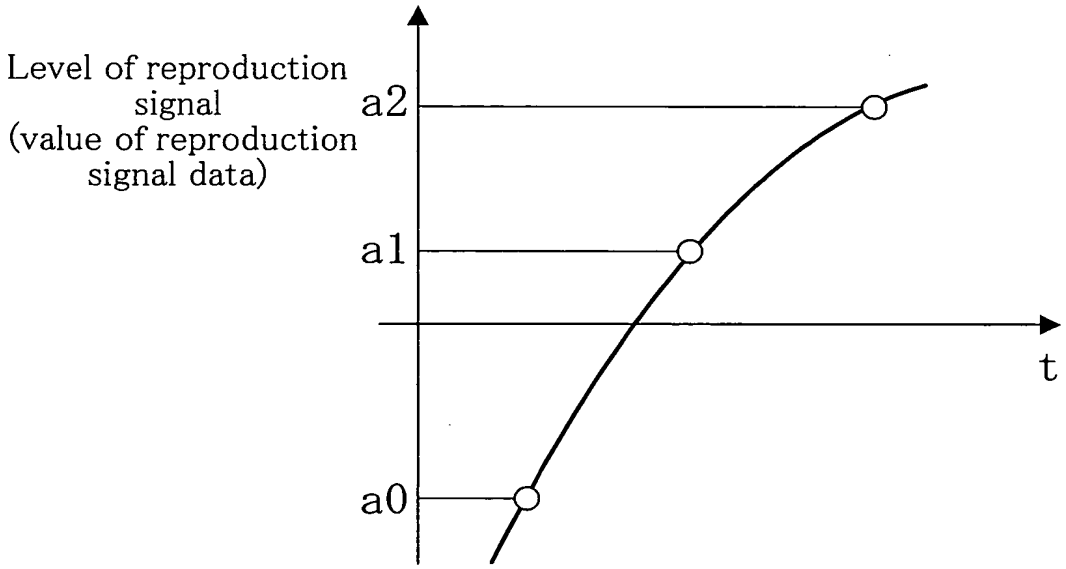

Level of reproduction signal (value of reproduction signal data)
a2
a1
a0
t

FIG. 8

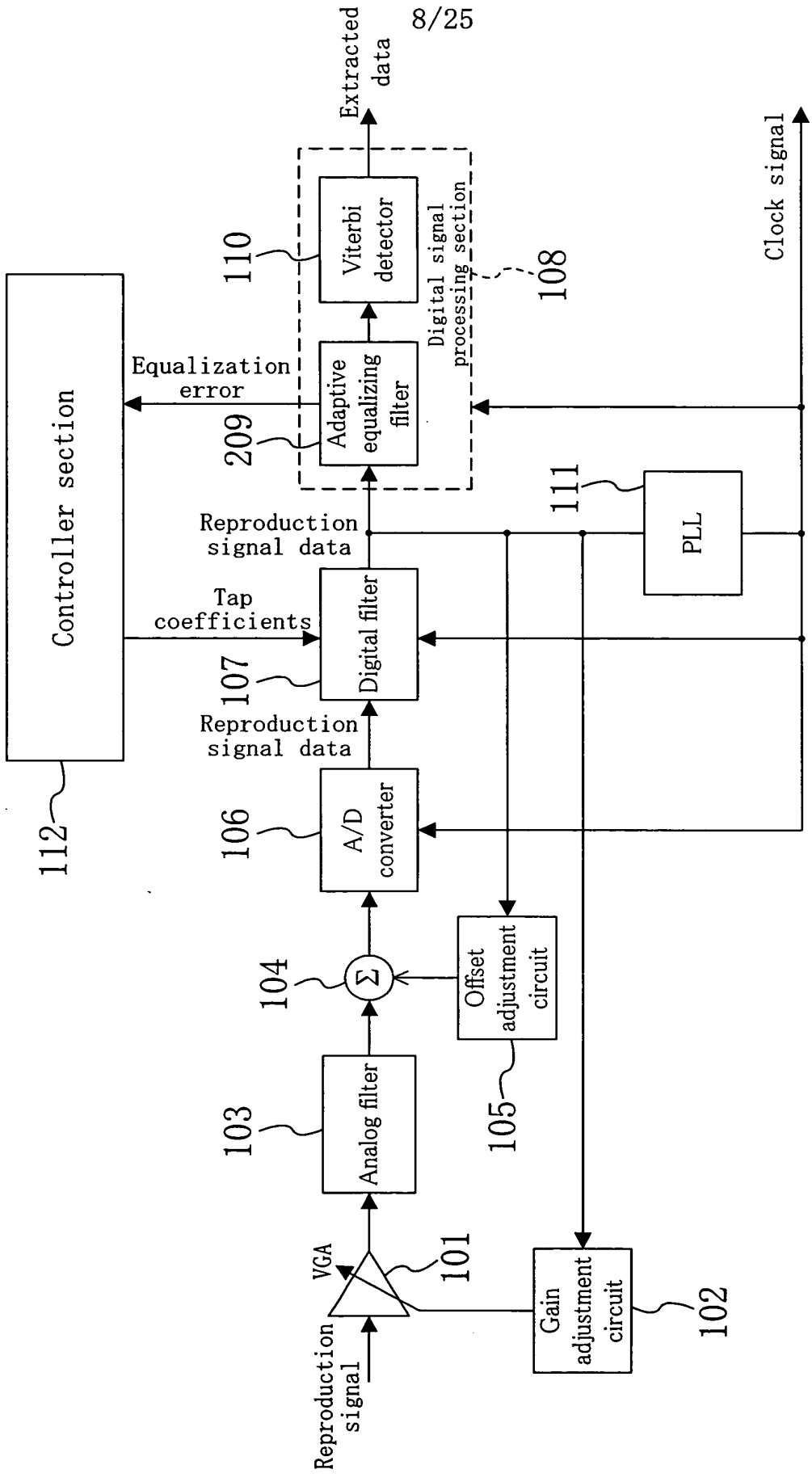

Extracted data
Viterbi detector
110
Digital signal processing section
108
Clock signal
Controller section
Equalization error
Adaptive equalizing filter
209
111
PLL
Reproduction signal data
Tap coefficients
Digital filter
107
Reproduction signal data
112
106
A/D converter
104
Σ
Offset adjustment circuit
103
Analog filter
105
VGA
101
Gain adjustment circuit
102
Reproduction signal

FIG. 9

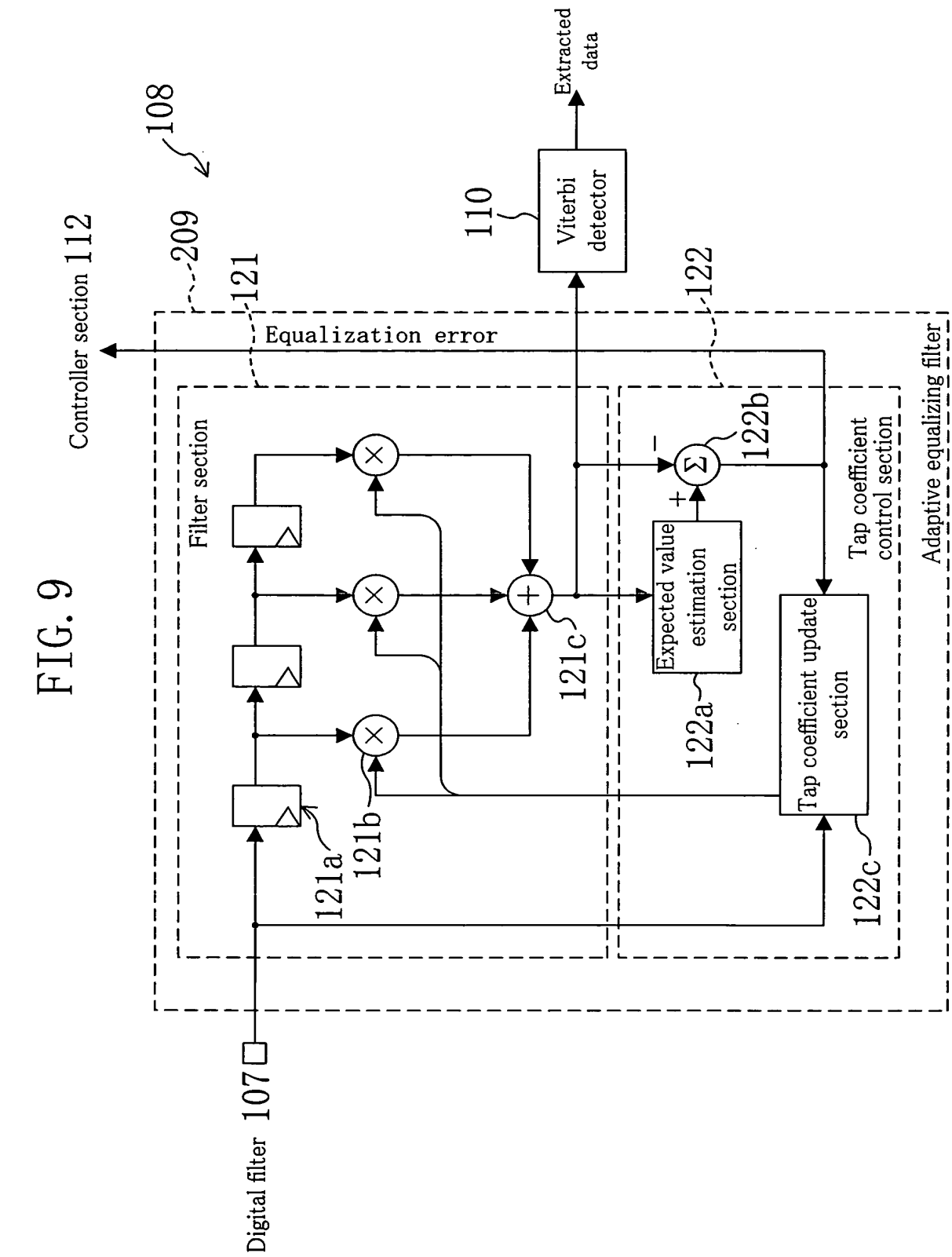

Digital filter
107
Controller section
112
108
209
121
Equalization error
Filter section
121a
121b
121c
110
Viterbi detector
Extracted data
122
122a
Expected value estimation section
122b
Σ
122c
Tap coefficient update section
Tap coefficient control section
Adaptive equalizing filter

FIG. 10

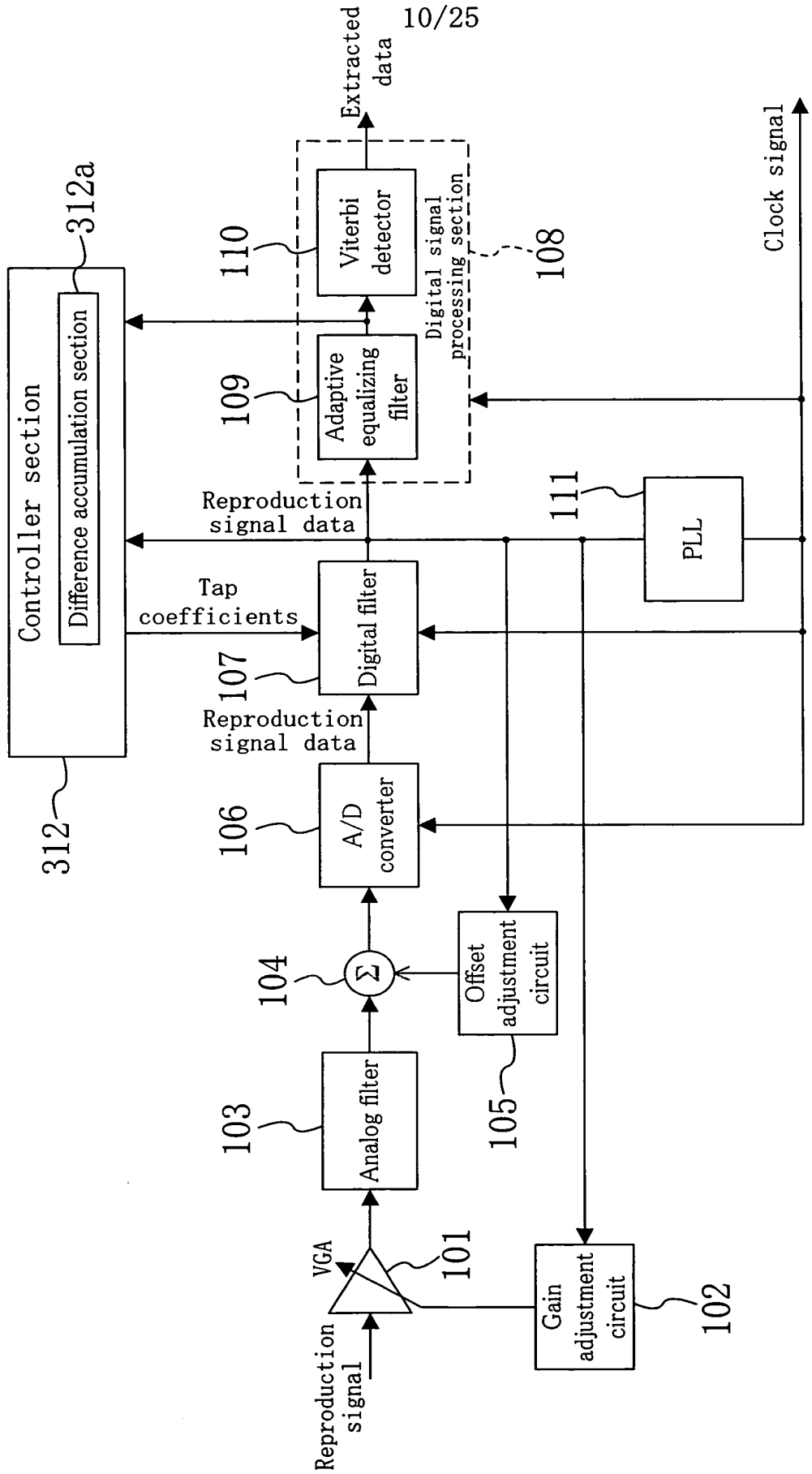

Extracted data
Clock signal
Viterbi detector
110
Digital signal processing section
108
Adaptive equalizing filter
109
312a
Controller section
Difference accumulation section
312
Reproduction signal data
111
PLL
Tap coefficients
Digital filter
107
Reproduction signal data
A/D converter
106
Offset adjustment circuit
104
105
Analog filter
103
VGA
101
Gain adjustment circuit
102
Reproduction signal

FIG. 11

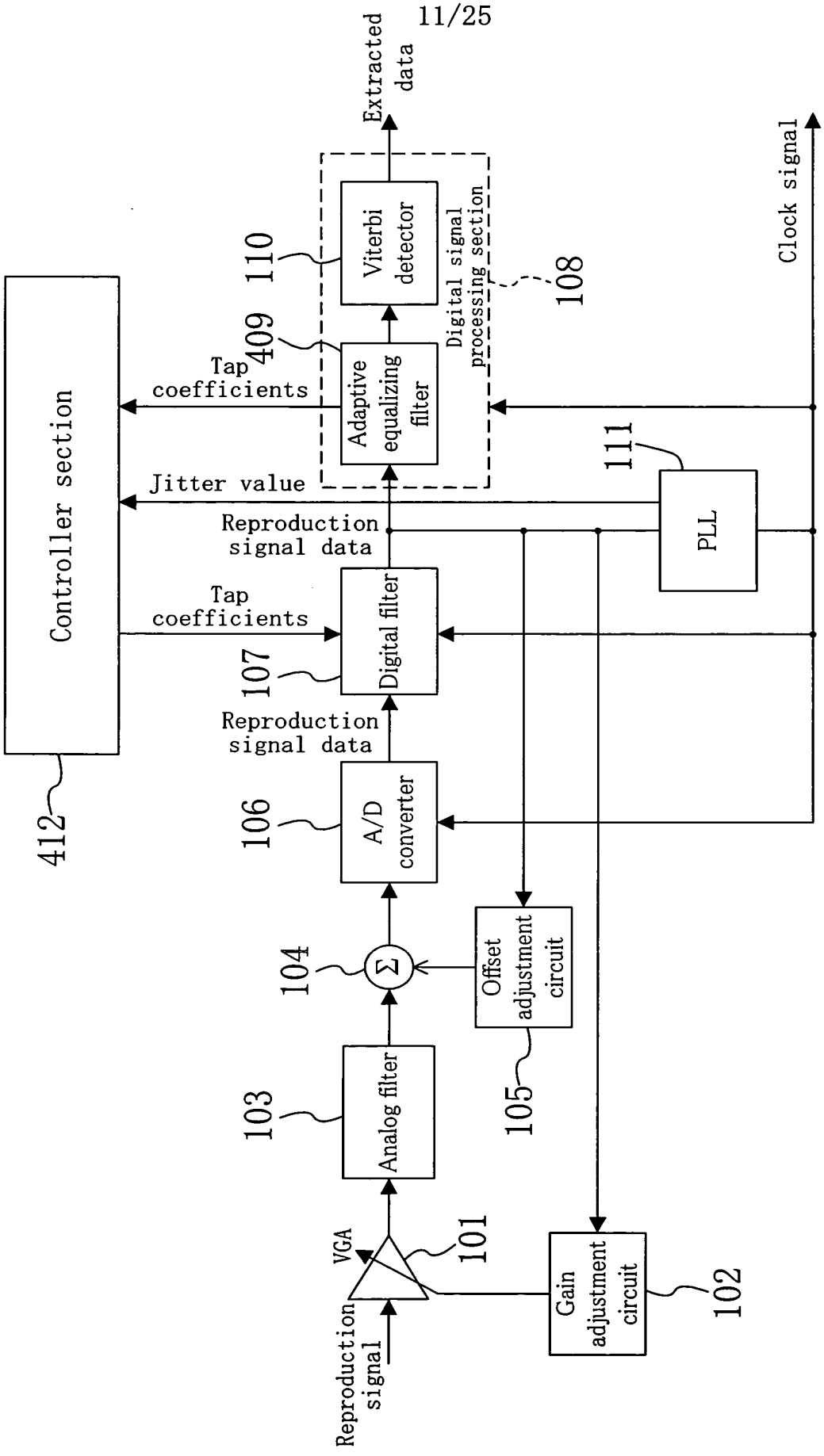

Reproduction signal
VGA
101
Gain adjustment circuit
102
Analog filter
103
Offset adjustment circuit
105
104
Σ
A/D converter
106
Digital filter
107
Reproduction signal data
Tap coefficients
Controller section
412
Jitter value
Reproduction signal data
Tap coefficients
409
Adaptive equalizing filter
Viterbi detector
110
Digital signal processing section
108
Extracted data
PLL
111
Clock signal

FIG. 12

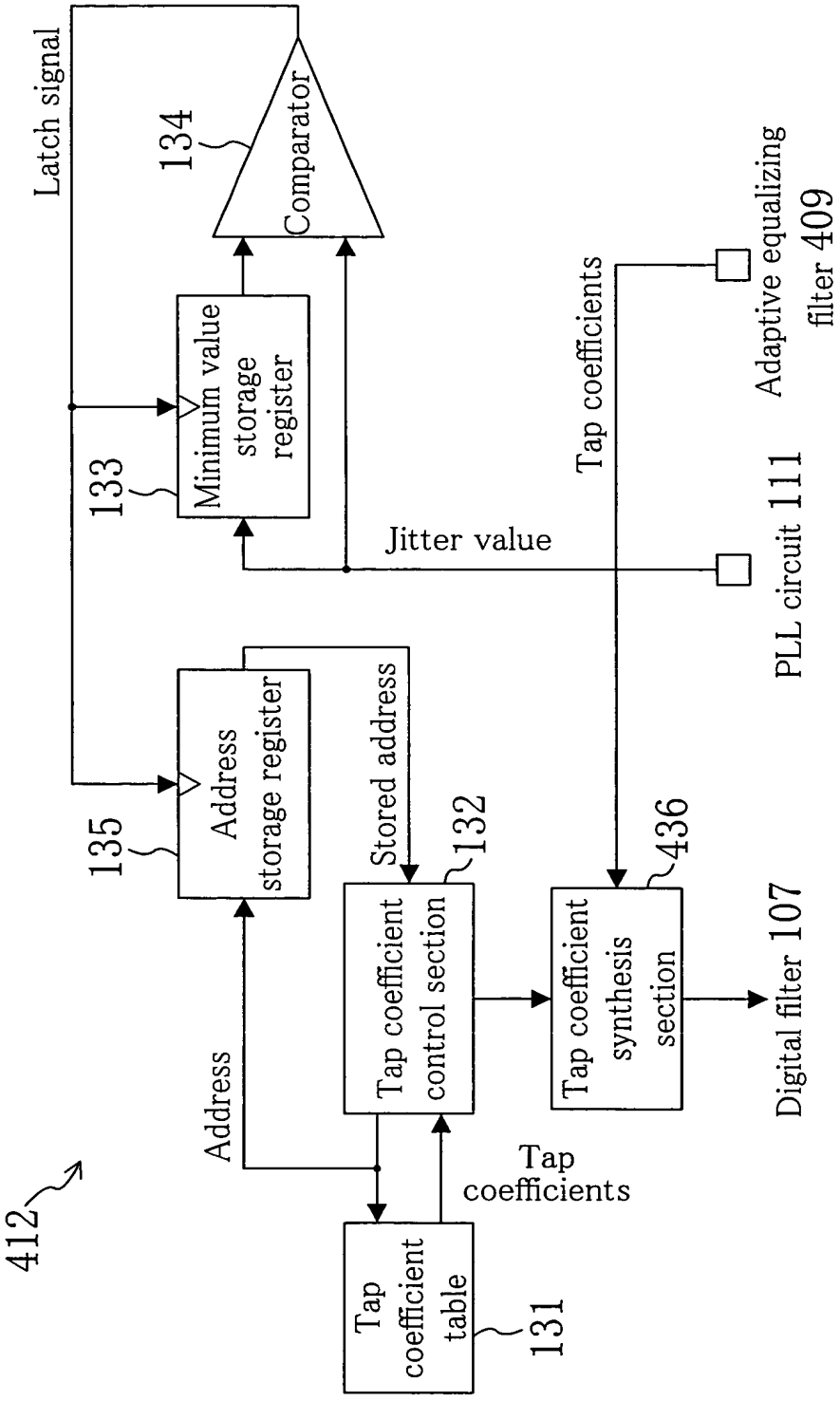

Latch signal
134
Comparator
Minimum value storage register
133
Jitter value
Tap coefficients
Adaptive equalizing filter 409
PLL circuit 111
Address storage register
135
Stored address
Tap coefficient control section
132
Tap coefficient synthesis section
436
Digital filter 107
Address
Tap coefficients
412
Tap coefficient table
131

FIG. 13

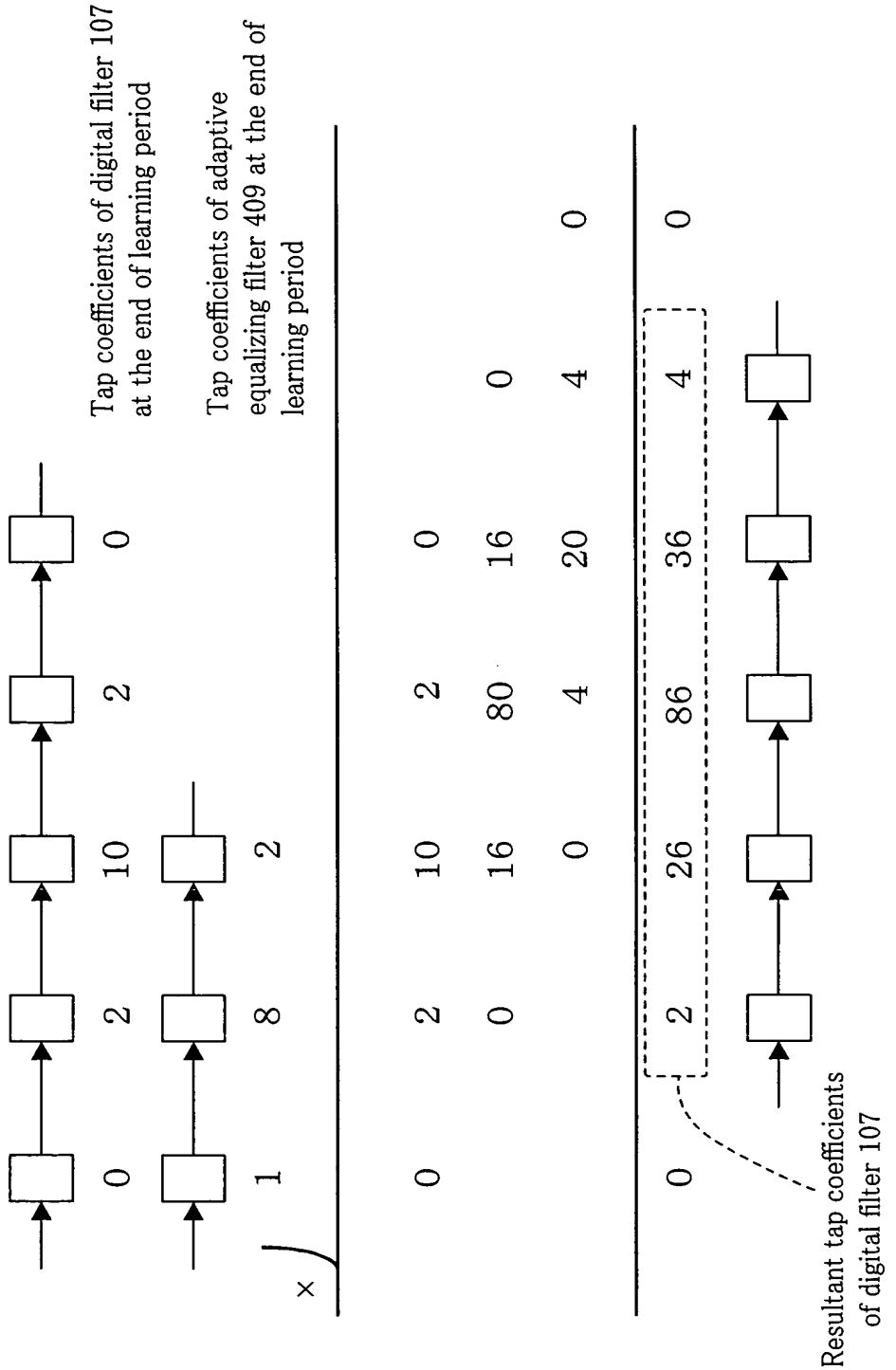

Tap coefficients of digital filter 107 at the end of learning period
Tap coefficients of adaptive equalizing filter 409 at the end of learning period
0 2 10 2 0
1 8 2
×
0 2 10 2 0
0 16 80 16 0
0 4 20 4 0
0 2 26 86 36 4 0
Resultant tap coefficients of digital filter 107

FIG. 14

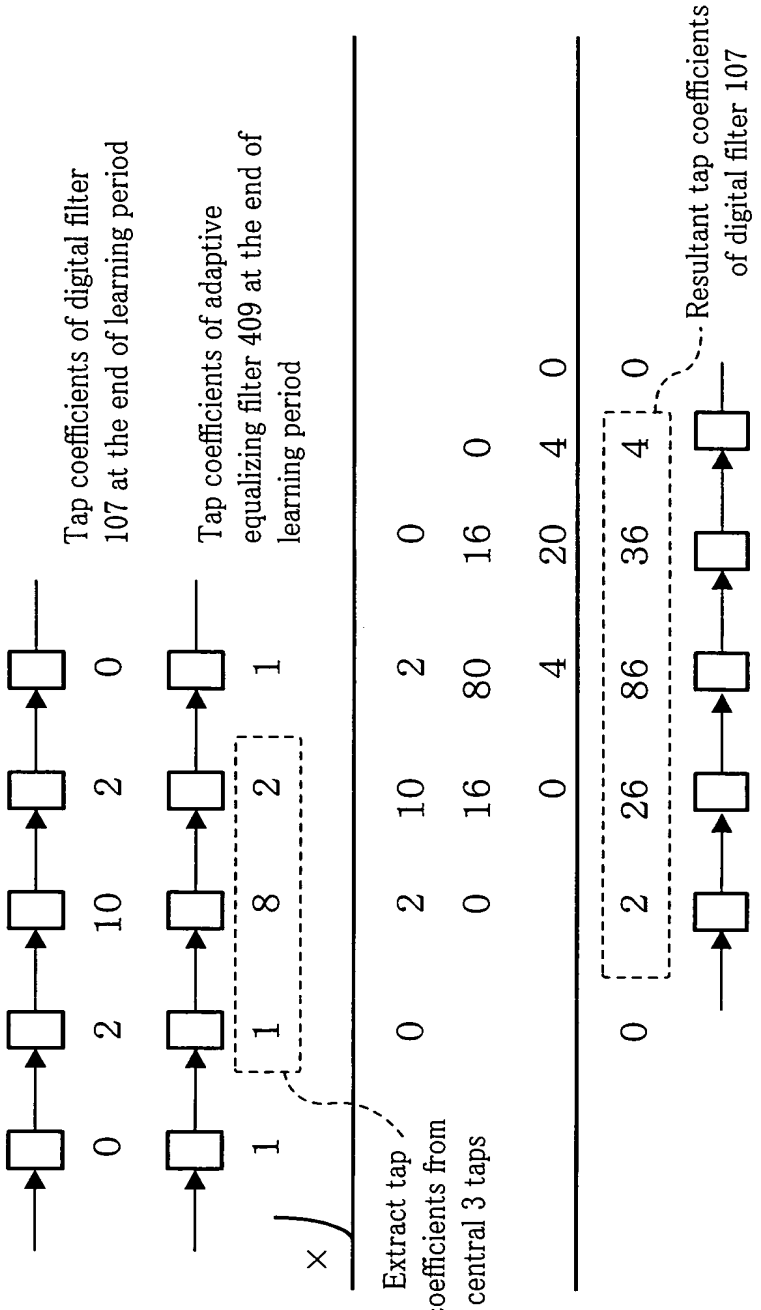

Tap coefficients of digital filter 107 at the end of learning period
0 2 10 2 0
Tap coefficients of adaptive equalizing filter 409 at the end of learning period
1 1 8 2 1
×
Extract tap coefficients from central 3 taps
0 2 10 2 0
0 16 80 16 0
0 4 20 4 0
0 2 26 86 36 4 0
Resultant tap coefficients of digital filter 107

FIG. 15

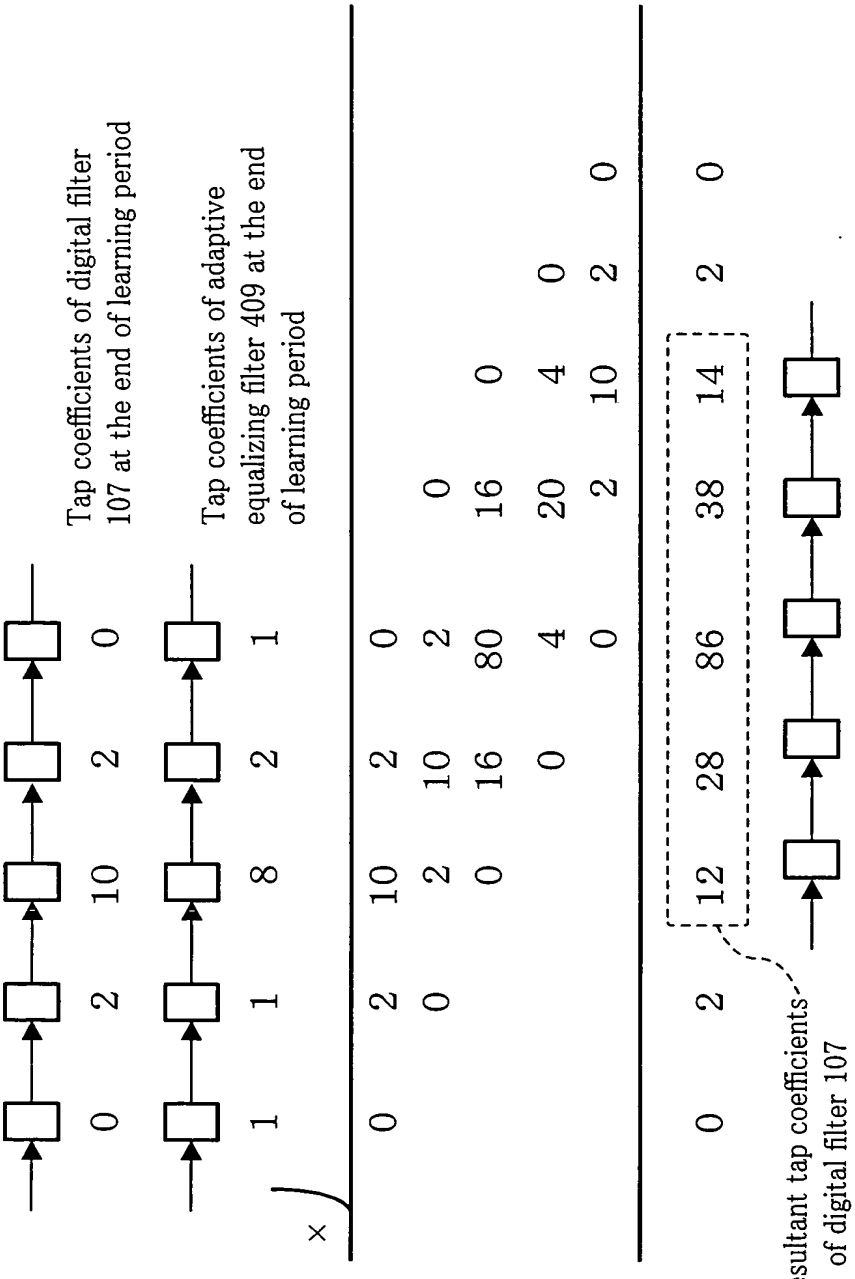

Tap coefficients of digital filter 107 at the end of learning period
0 2 10 2 0
Tap coefficients of adaptive equalizing filter 409 at the end of learning period
1 1 8 2 1
×
0 2 10 2 0
0 2 10 2 0
0 16 80 16 0
0 4 20 4 0
0 2 10 2 0
0 2 12 28 86 38 14 2 0
Resultant tap coefficients of digital filter 107

FIG. 16

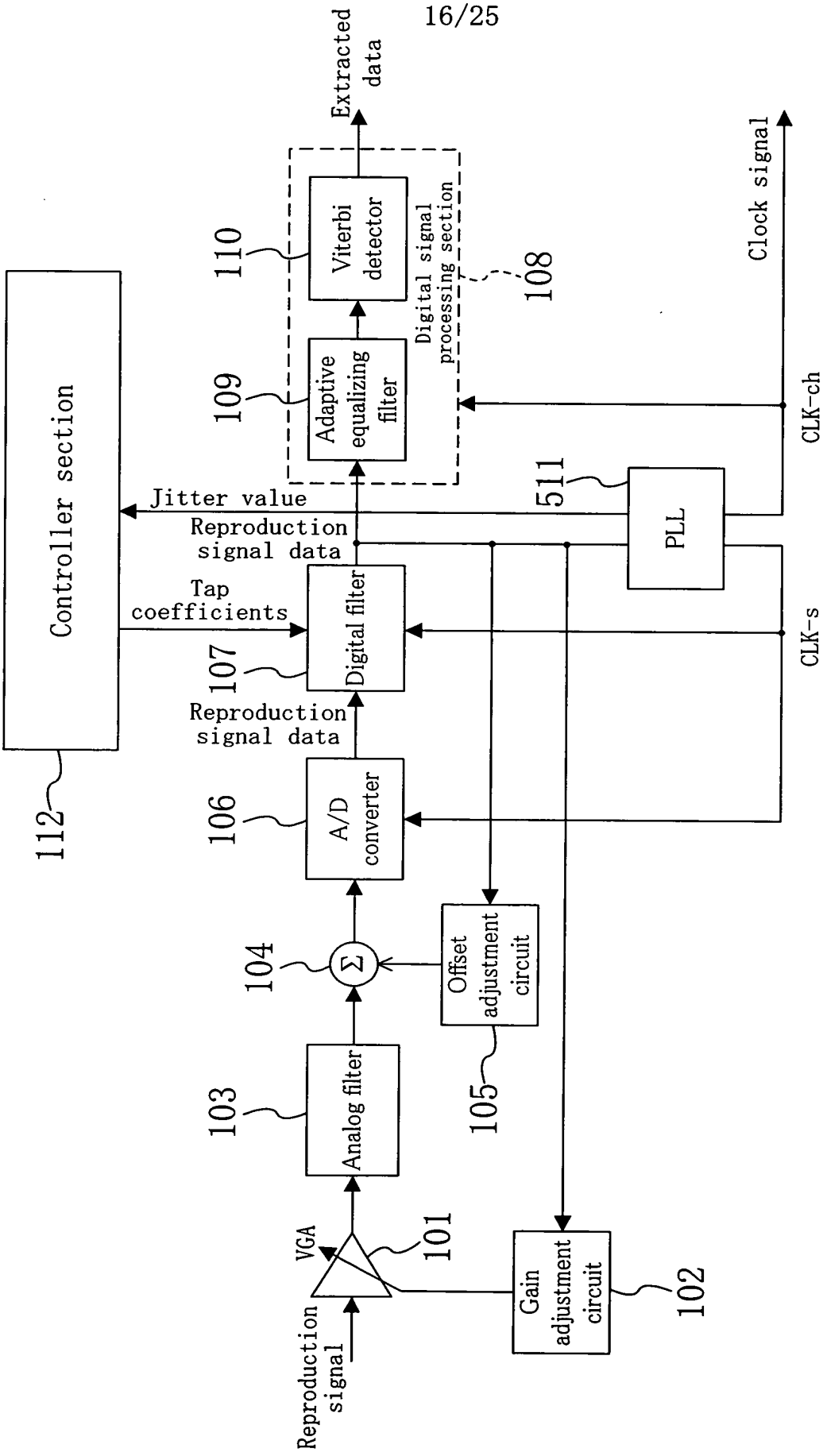

Extracted data
Viterbi detector
110
Digital signal processing section
108
Adaptive equalizing filter
109
Clock signal
CLK-ch
Controller section
Jitter value
Reproduction signal data
511
PLL
Tap coefficients
Digital filter
107
CLK-s
Reproduction signal data
A/D converter
106
112
104
Offset adjustment circuit
105
Analog filter
103
VGA
101
Gain adjustment circuit
102
Reproduction signal

FIG. 17

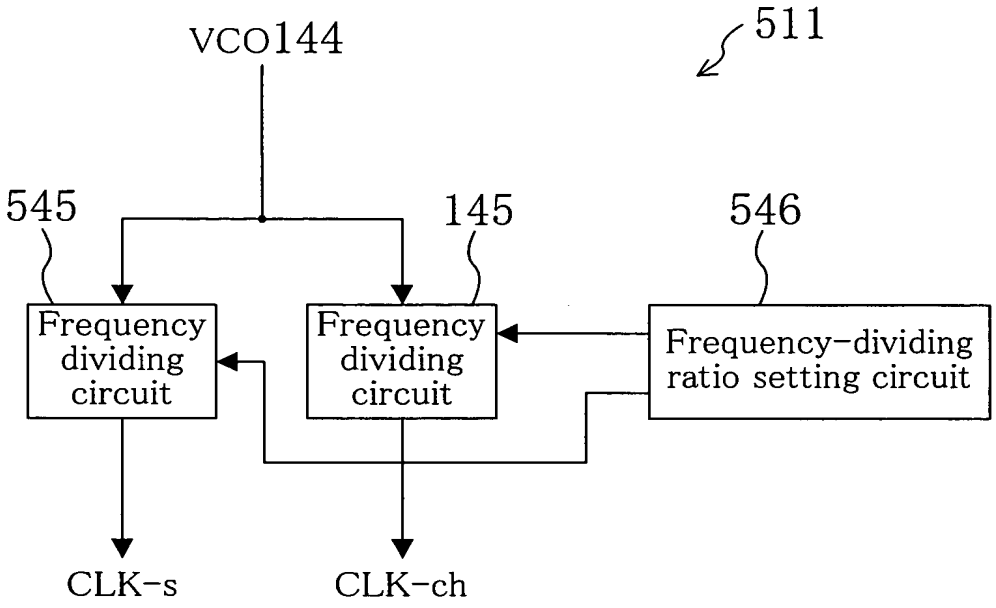

VCO144
511
545
145
546
Frequency dividing circuit
Frequency dividing circuit
Frequency-dividing ratio setting circuit
CLK-s
CLK-ch

FIG. 18

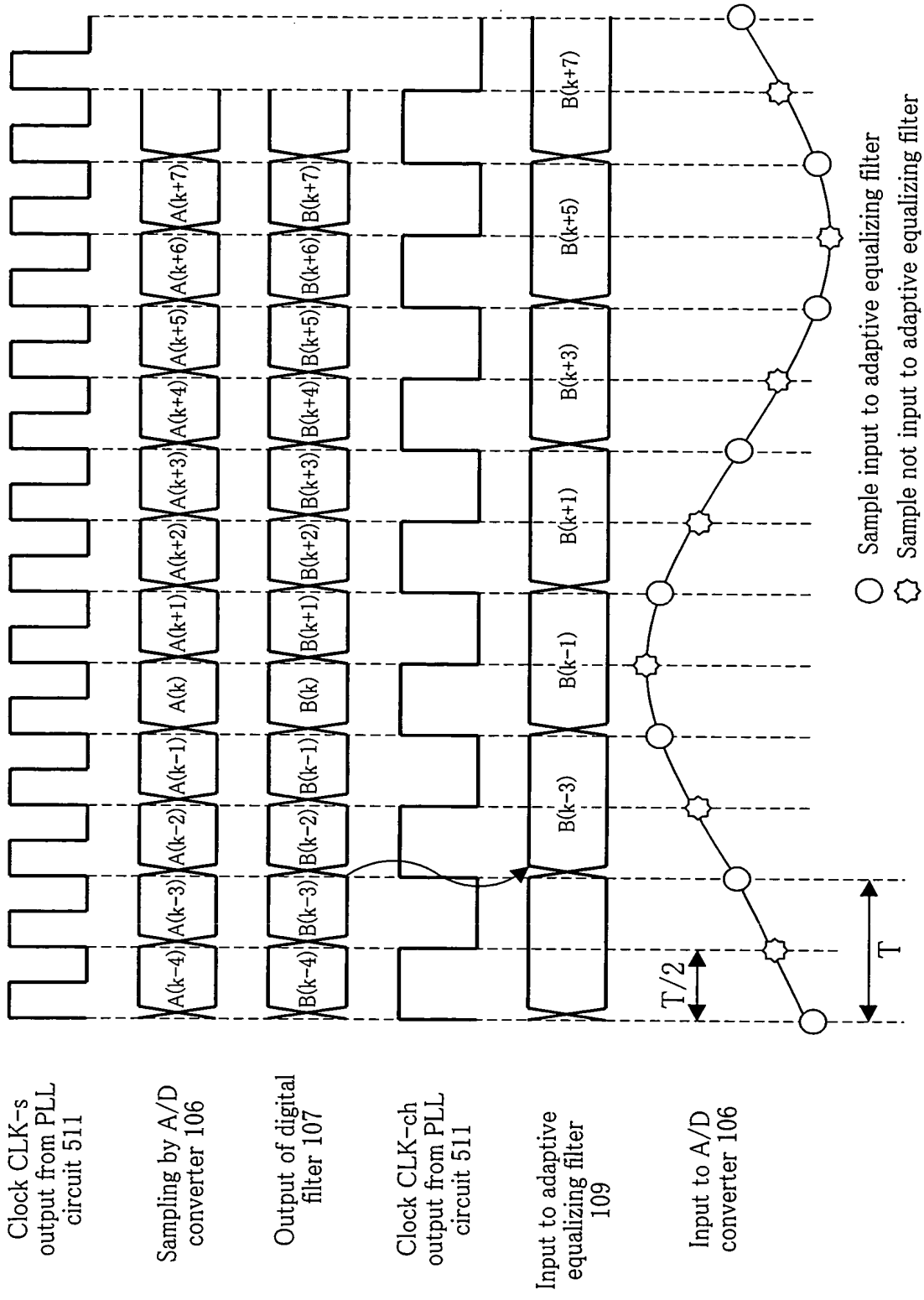

Clock CLK-s output from PLL circuit 511
Sampling by A/D converter 106
Output of digital filter 107
Clock CLK-ch output from PLL circuit 511
Input to adaptive equalizing filter 109
Input to A/D converter 106
A(k-4)
A(k-3)
A(k-2)
A(k-1)
A(k)
A(k+1)
A(k+2)
A(k+3)
A(k+4)
A(k+5)
A(k+6)
A(k+7)
B(k-4)
B(k-3)
B(k-2)
B(k-1)
B(k)
B(k+1)
B(k+2)
B(k+3)
B(k+4)
B(k+5)
B(k+6)
B(k+7)
B(k-3)
B(k-1)
B(k+1)
B(k+3)
B(k+5)
B(k+7)
T/2
T
Sample input to adaptive equalizing filter
Sample not input to adaptive equalizing filter

FIG. 19

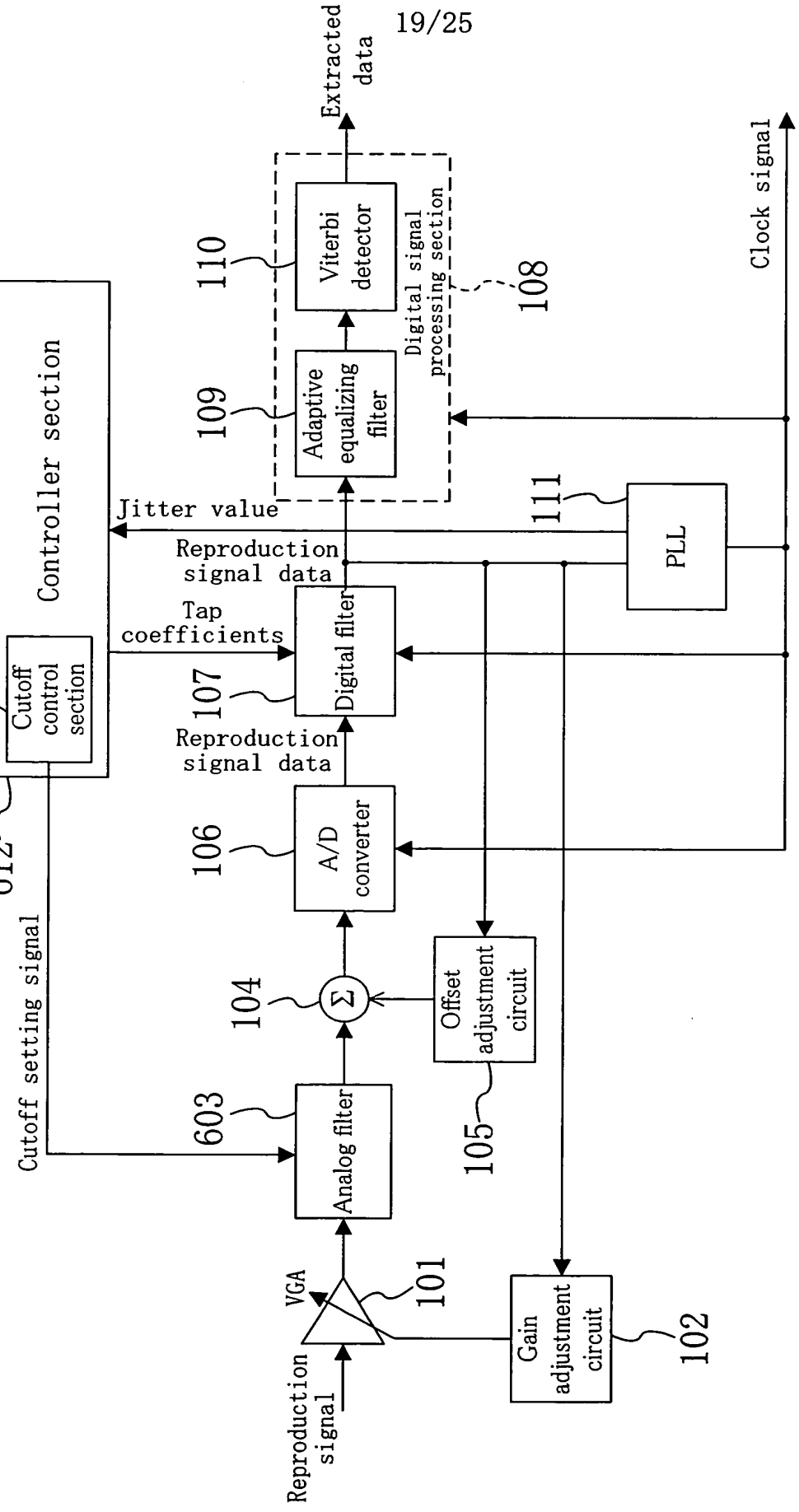
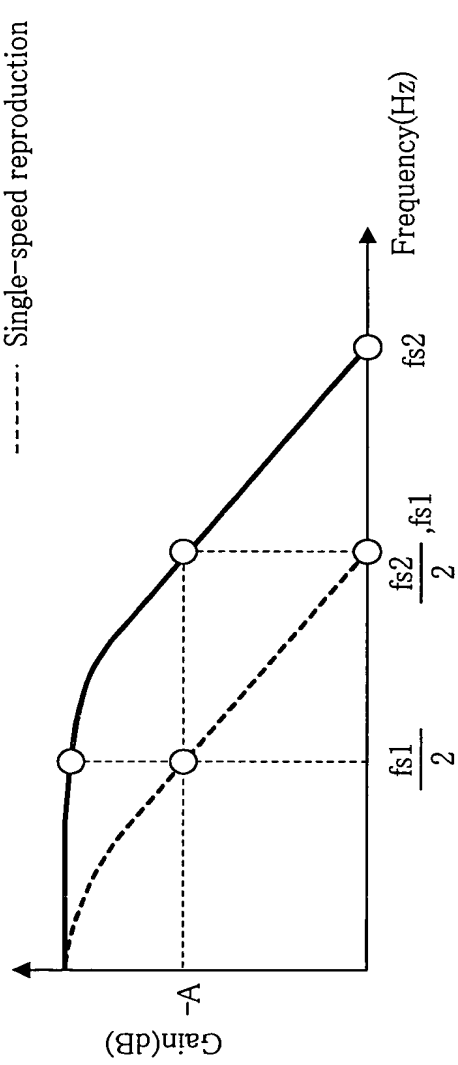

Reproduction signal
VGA
101
Gain adjustment circuit
102
Analog filter
603
Offset adjustment circuit
105
Σ
104
A/D converter
106
Digital filter
107
Reproduction signal data
Tap coefficients
Cutoff control section
612a
Controller section
612
Cutoff setting signal
Jitter value
Reproduction signal data
Adaptive equalizing filter
109
Viterbi detector
110
Digital signal processing section
108
Extracted data
PLL
111
Clock signal

FIG. 20



fs2 Sampling clock frequency in double-speed reproduction

fs1 Sampling clock frequency in single-speed reproduction

FIG. 21

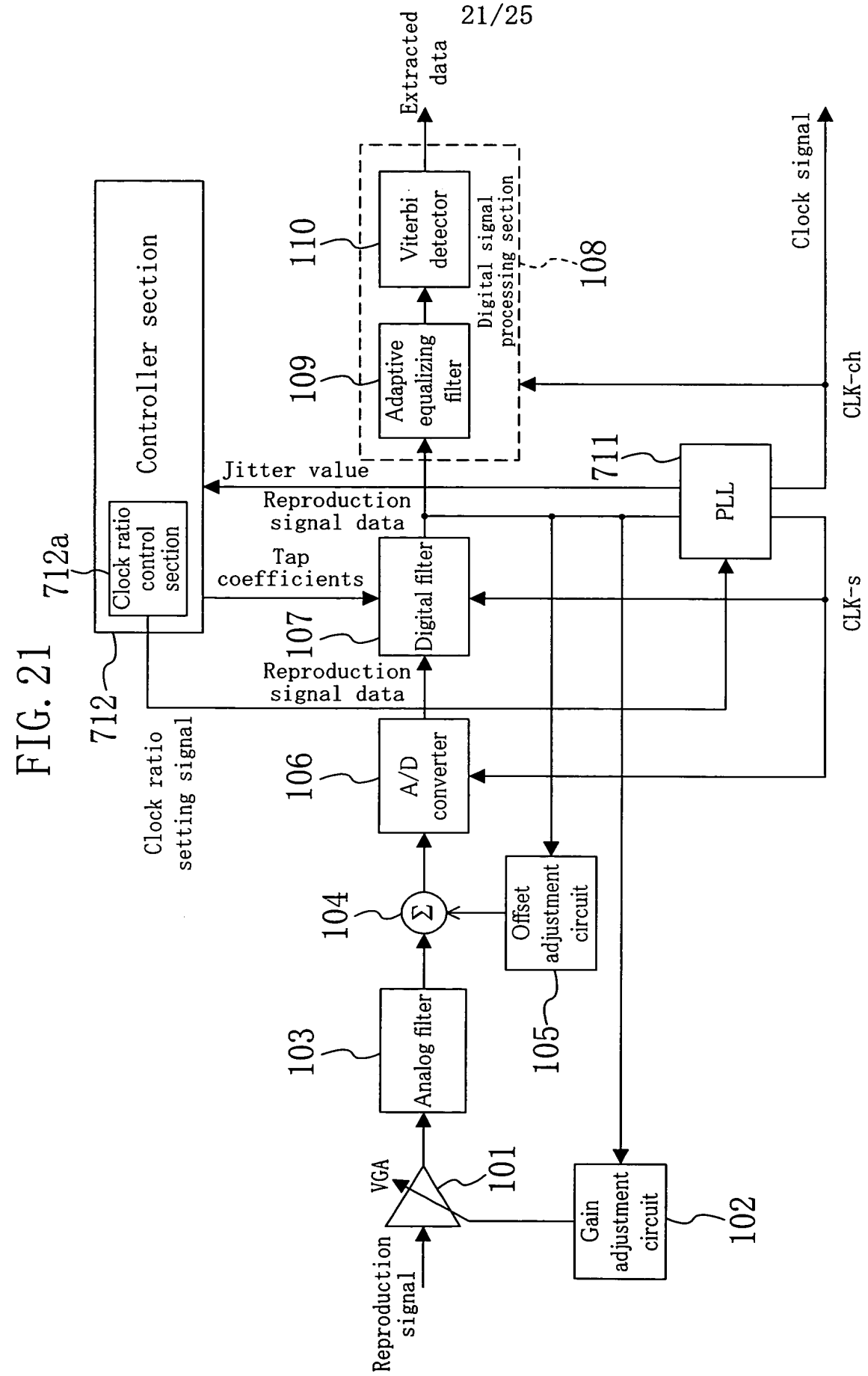

Reproduction signal
VGA
101
Gain adjustment circuit
102
Analog filter
103
105
Offset adjustment circuit
104
Σ
A/D converter
106
Clock ratio setting signal
712
712a
Clock ratio control section
Controller section
Tap coefficients
Digital filter
107
Reproduction signal data
Reproduction signal data
Jitter value
Adaptive equalizing filter
109
Viterbi detector
110
Digital signal processing section
108
Extracted data
PLL
711
CLK-s
CLK-ch
Clock signal

FIG. 22

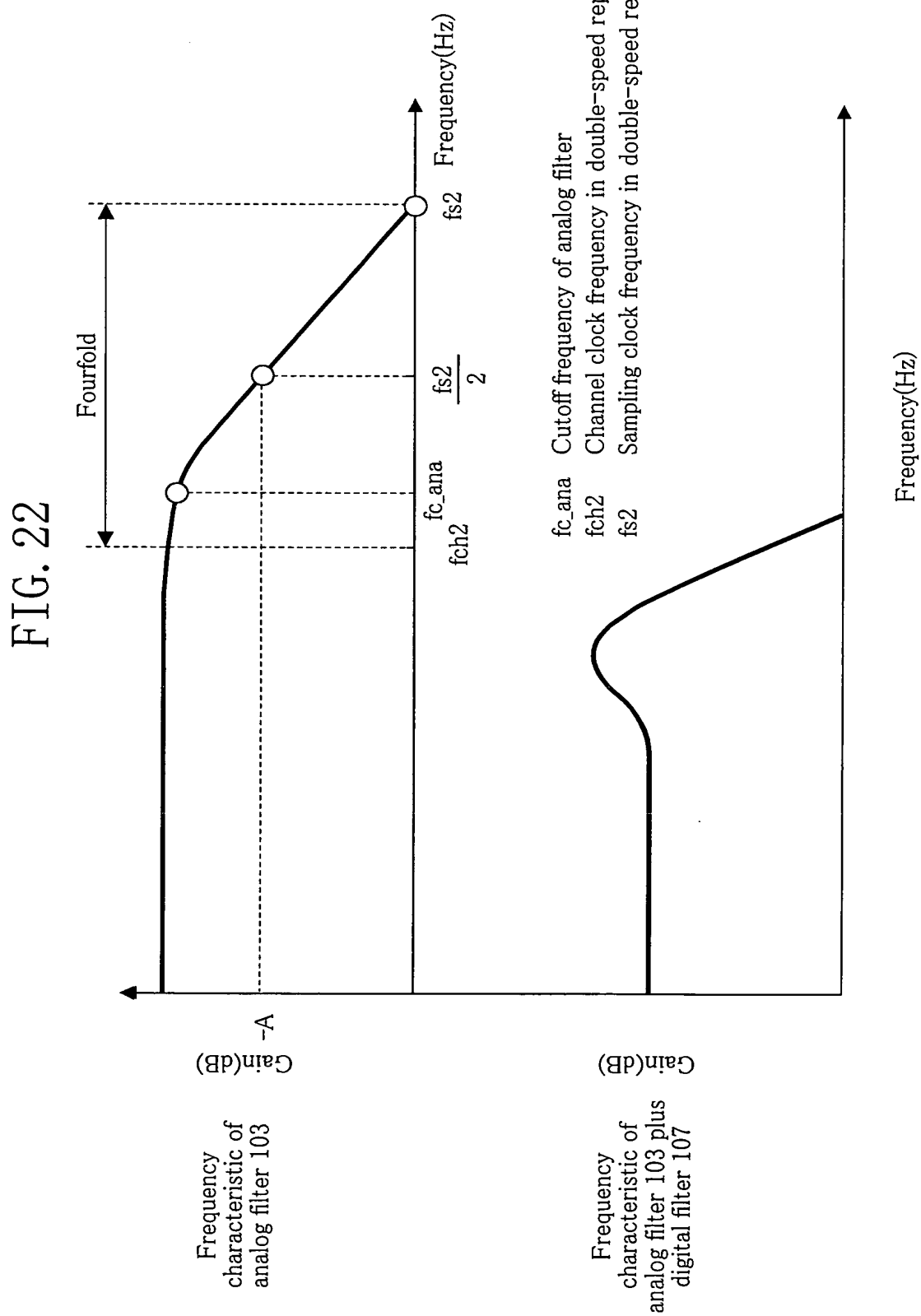

Frequency characteristic of analog filter 103
Gain(dB)
-A
Frequency(Hz)
Fourfold
fs2
fs2/2
fc_ana
fch2
Frequency characteristic of analog filter 103 plus digital filter 107
Gain(dB)
Frequency(Hz)
fc_ana Cutoff frequency of analog filter
fch2 Channel clock frequency in double-speed reproduction
fs2 Sampling clock frequency in double-speed reproduction

FIG. 23

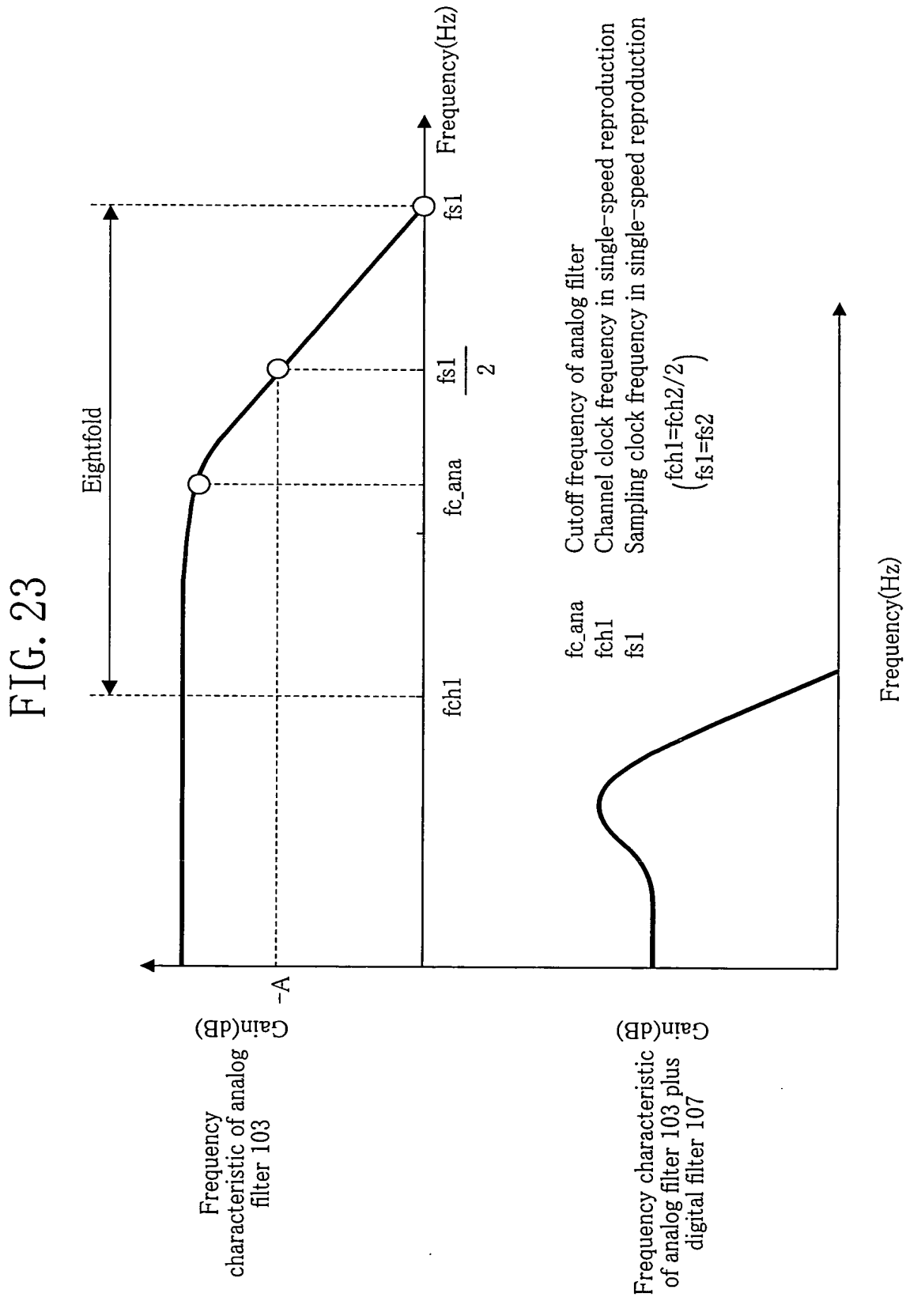

Frequency characteristic of analog filter 103
Gain(dB)
-A
Eightfold
fch1
fc_ana
fs1/2
fs1
Frequency(Hz)
Frequency characteristic of analog filter 103 plus digital filter 107
Gain(dB)
fc_ana Cutoff frequency of analog filter
fch1 Channel clock frequency in single-speed reproduction
fs1 Sampling clock frequency in single-speed reproduction
(fch1=fch2/2
fs1=fs2)
Frequency(Hz)

FIG. 24

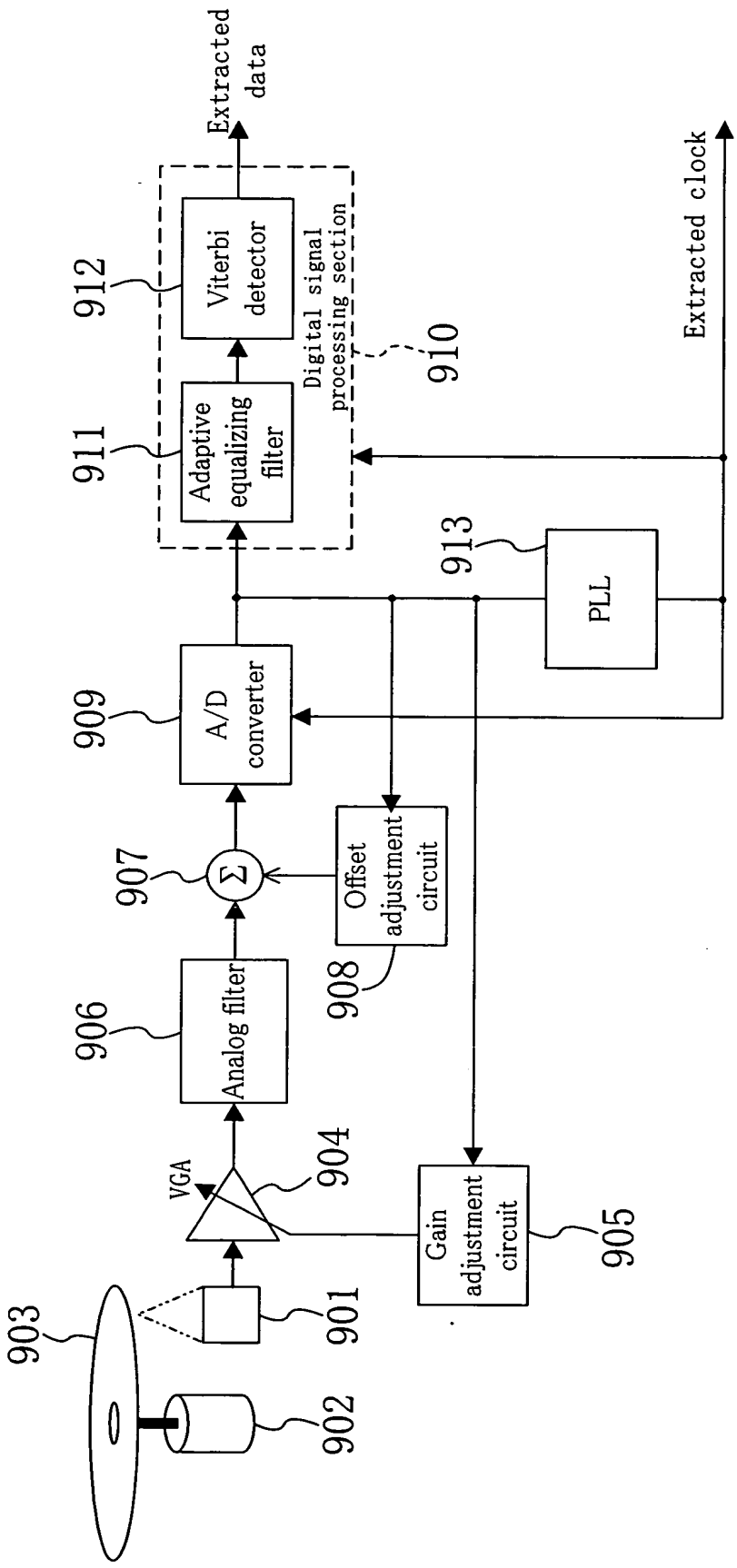
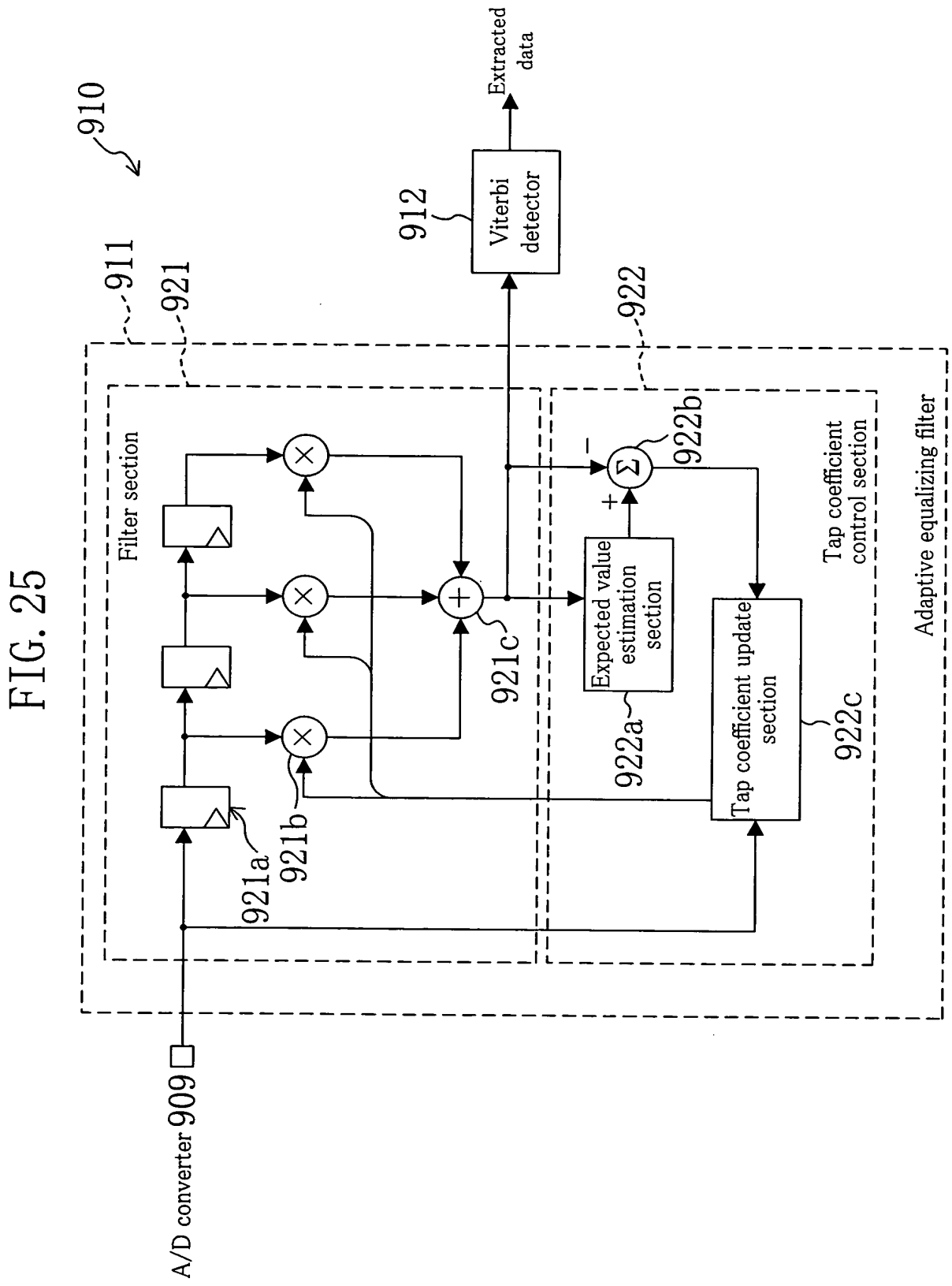

Extracted data
Viterbi detector
912
Digital signal processing section
910
Adaptive equalizing filter
911
Extracted clock
913
PLL
A/D converter
909
Offset adjustment circuit
908
907
Σ
Analog filter
906
VGA
904
Gain adjustment circuit
905
903
901
902

FIG. 25


910
911
921
922
912
Viterbi detector
Extracted data
Filter section
Tap coefficient control section
Adaptive equalizing filter
921a
921b
921c
922a
922b
922c
Expected value estimation section
Tap coefficient update section
A/D converter 909